IN THE SPECIFICATION:

Paragraph beginning at line 2 of page 1 has been amended as follows:

The present invention relates to a manufacturing method for a CMOS semiconductor device having a ~~dual-gate~~ bipolar gate structure, which enables a low-voltage operation and low power consumption.

Paragraph beginning at line 5 of page 1 has been amended as follows:

To enable the low-voltage operation of the semiconductor device, it is necessary to form both of an NMOS and a PMOS constituting the CMOS as surface-channel type elements. Here, for explaining a manufacturing method for a conventional ~~dual-gate~~ bipolar gate CMOS semiconductor device, with which the above structure is achieved, a half-completed structure in its production is shown in Fig. 8. An N-well region 202 is partially formed with a boundary defined by a field insulation film 203 formed on a P-type semiconductor substrate 201. A gate insulating film 204 is formed on the P-type semiconductor substrate 201 and the N-well region 202. Then, a polycrystalline silicon film 205 is formed on top thereof. A P-type polycrystalline silicon film region 207 is

formed by implanting boron ions using as a mask a resist patterned so as to open a region serving as the PMOS, onto the polycrystalline silicon. Subsequently, an N-type polycrystalline silicon film region 206 is formed by implanting phosphorous ions using as a mask a resist patterned so as to open a region serving as the NMOS (see, for example, Patent Document 1). Also, there is known a forming method capable of achieving the structure of Fig. 8, in which the boron ions are previously implanted into the entire polycrystalline silicon to form the P-type polycrystalline silicon region, after which the phosphorous ions are implanted using as the mask the resist patterned so as to open the region serving as the NMOS, and the N-type polycrystalline silicon region 206 is formed through counter-doping of the phosphorous into the P-type polycrystalline silicon region (see, for example, Patent Document 1).

Paragraph beginning at line 10 of page 8 has been amended as follows:

Subsequently, after the photoresist 107 is removed, through the so-called predeposition for doping the impurity by heat treatment in a diffusion furnace in an N-type impurity atmosphere, the polycrystalline silicon except for the region where the insulating film 106 is formed is changed into an N+

polycrystalline silicon 108 to thereby obtain a structure shown in Fig. 4. The impurity is only doped into a portion where the polycrystalline silicon is exposed and thus, is not doped into a region covered with the insulating film. As the impurity in this case, phosphorous is used, which is widely employed in the predeposition.